What is claimed is:

1. In a phase-locked loop (PLL) disposed on a circuit chip and including a synthesizer, a voltage-controlled oscillator (VCO) calibration system disposed on the circuit chip comprising:

an input configured to receive a tuning voltage;

a plurality of VCOs in a set of VCOs, each VCO including a plurality of selectively coupled varactors;

a tuning-voltage-distribution circuit configured to couple the input to the VCOs; and

a calibration circuit coupled to at least one of the power distribution circuit and the set of VCOs and configured to control tuning voltage distribution from the input to selective varactors of each VCO, to determine a selected VCO of the set of VCOs that is capable of producing a desired range of frequencies in response to tuning voltages within a desired range of tuning voltages, and to determine a desired combination of the varactors to use in the selected VCO to produce the desired range of frequencies in response the tuning voltages within the desired range of tuning voltages.

2. The system of claim 1 wherein the calibration circuit is further configured to set the synthesizer to an extreme-frequency channel, and to control the distribution

circuit to provide the tuning voltage to a combination of varactors providing an extreme capacitance for each VCO.

3. The system of claim 2 wherein the calibration circuit is further configured to control a portion of the set of VCOs to produce an output frequency corresponding to the extreme-frequency channel, and to determine the selected VCO based on a level of the tuning voltage used by each VCO, in the portion of VCOs, to produce the output frequency.

4. The system of claim 3 wherein the calibration circuit is further configured to determine the selected VCO in response to whether the level of the tuning voltage used by each VCO, in the portion of VCOs, to produce the output frequency is in a range from a minimum tuning voltage to a maximum tuning voltage.

5. The system of claim 4 wherein the calibration circuit is further configured to determine the selected VCO in response to whether the level of the tuning voltage used by each VCO, in the portion of VCOs, to produce the output frequency is in an effective range of acceptable tuning voltages.

6. The system of claim 2 wherein the extreme-frequency channel is the lowest-frequency channel, and the extreme capacitance is the lowest capacitance amount available for each VCO.

7. The system of claim 1 wherein the calibration circuit is configured to set the synthesizer to an extreme-frequency channel, and to determine the desired combination of the varactors by adjusting which varactors of the selected VCO receive the tuning voltage and determining whether a level of the tuning voltage used by the selected VCO to produce an output frequency corresponding to the extreme-frequency channel is within the desired range of tuning voltages.

8. The system of claim 7 wherein the desired range of tuning voltages is an effective range of acceptable tuning voltages.

9. A circuit chip comprising:

a first portion of a phase-locked loop circuit; and

a second portion of a phase-locked loop circuit coupled to the first portion of the phase-locked loop circuit and comprising a voltage-controlled oscillator (VCO) calibration system comprising:

an input configured to receive a tuning voltage;

a plurality of VCOs each including a plurality of selectively coupled varactors;

a tuning voltage distribution circuit configured to couple the input to a selected VCO and a selected combination of varactors of the selected VCO;

a voltage range indicator circuit coupled to the input and configured to provide indicia of whether the tuning voltage is within a desired range; and

a calibration circuit coupled to the input, the tuning voltage distribution circuit, and the voltage range indicator circuit, and configured to control the tuning voltage distribution circuit to control distribution of the tuning voltage to selective varactors of each VCO, to determine a selected VCO that is capable of producing a desired range of frequencies in response to tuning voltages within the desired range of tuning voltages, and to determine a desired combination of the varactors to use in the selected VCO to produce the desired range of frequencies in response the tuning voltages within the desired range of tuning voltages.

10. The circuit chip of claim 9 wherein the first portion of the phase-locked loop circuit includes a synthesizer and the calibration circuit is configured to set the synthesizer to an extreme-frequency channel, to control the tuning voltage distribution circuit to provide the tuning voltage to a combination of varactors providing an extreme capacitance for the selected VCO, and to determine the desired combination of the

varactors by adjusting which varactors of the selected VCO receive the tuning voltage and determining whether a level of the tuning voltage used by the selected VCO to produce an output frequency corresponding to the extreme-frequency channel is within the desired range of tuning voltages.

11. The circuit chip of claim 10 wherein the voltage range indicator circuit comprises a low-voltage determining circuit, a high-voltage determining circuit, and a voltage-tolerance circuit, and wherein outputs from the low-voltage determining circuit, high-voltage determining circuit, and voltage-tolerance circuit indicate whether a given tuning voltage is within the desired range of tuning voltages.

12. The circuit chip of claim 11 wherein the desired range of tuning voltage is an effective range of acceptable tuning voltages.

13. In a phase-locked loop (PLL) disposed on a circuit chip and including a synthesizer, an on-chip voltage-controlled oscillator (VCO) calibration system comprising:

an input configured to receive a tuning voltage;

a switch configured to selectively couple the input to respective ones of a plurality of first lines in response to a switch control signal;

a plurality of multiplexers coupled to respective first lines and each configured to connect its respective first line to a plurality of second lines in response to a multiplexer control signal;

a plurality of VCOs corresponding to the plurality of first lines, each VCO including a fine varactor coupled to the respective first line, each VCO further including a plurality of coarse varactors coupled to a respective plurality of second lines;

a hysteresis comparator coupled to the input and configured to compare the tuning voltage with a hysteresis reference voltage and to provide a hysteresis output indicative of the comparison of the tuning voltage and the hysteresis reference voltage;

a high-voltage comparator coupled to the input and configured to compare the tuning voltage with a high reference voltage and to provide a first output indicative of the comparison of the input voltage and the high reference voltage;

a low-voltage comparator coupled to the input and configured to compare the tuning voltage with a low reference voltage and to provide a second output indicative of the comparison of the input voltage and the low reference voltage; and

a calibration circuit, coupled to the switch, the multiplexers, the hysteresis comparator, the high-voltage comparator, the low-voltage comparator, and at least one of the power distribution circuit and the set of VCOs, for providing the switch control signal and the multiplexer control signals, for controlling tuning voltage distribution from the input to selective ones of the varactors of each VCO, determining a selected VCO from

the plurality of VCOs that is capable of producing a desired range of frequencies in response to tuning voltages within a desired range of tuning voltages, and determining a desired combination of the varactors to use in the selected VCO to produce the desired range of frequencies in response the tuning voltages within the desired range of tuning voltages.

14. The system of claim 13 wherein the calibration circuit is configured to determine the selected VCO in response to the first and second outputs, and the tuning voltage.

15. The system of claim 14 wherein the calibration circuit is configured to determine the desired combination of varactors in response to the hysteresis output and at least one of the first and second outputs.

16. A calibration method for selecting a voltage-controlled oscillator (VCO), from a plurality of VCOs, and a varactor configuration for the selected VCO, to provide frequencies for a phase-locked loop (PLL) to use to lock to a plurality of channels having a corresponding plurality of frequencies, the method comprising:

setting a channel of the PLL to an extreme-frequency channel of the plurality of channels, the extreme-frequency channel being a channel having one of a highest-

corresponding frequency and a lowest-corresponding frequency of the corresponding plurality of frequencies;

providing, one VCO at a time, power and a tuning voltage to an extreme-capacitance combination of varactors of at least one of the VCOs, the extreme varactor combination providing one of a highest-capacitance amount available and a lowest-capacitance amount available;

allowing the tuning voltage provided to a VCO of the at least one of the VCOs, that is currently receiving power and the tuning voltage, to settle to a first settled tuning voltage;

determining whether the first settled tuning voltage is within an acceptable range of tuning voltages;

selecting a VCO whose corresponding first settled tuning voltage is within the acceptable range of voltages;

determining a desired combination of varactors for the selected VCO such that the selected VCO can provide frequencies associated with the plurality of frequencies corresponding to the plurality of channels with a second settled tuning voltage being within the acceptable range of voltages.

17. The method of claim 16 wherein determining the desired combination of varactors includes changing combinations of varactors of the selected VCO that receive the tuning voltage.

18. The method of claim 17 wherein changing combinations of varactors that receive the tuning voltage causes capacitance of the varactor combinations to change in a consecutively decreasing manner of available capacitances.

19. The method of claim 18 wherein the desired combination is the combination that provides the lowest available capacitance with the second settled tuning voltage being within the acceptable range.

20. The method of claim 17 wherein changing combinations of varactors that receive the tuning voltage causes capacitance of the varactor combinations to change in a consecutively increasing manner of available capacitances.

21. The method of claim 20 wherein the desired combination is the combination that provides the highest available capacitance with the second settled tuning voltage being within the acceptable range.

22. The method of claim 16 wherein the acceptable range is an effective acceptable range.

23. The method of claim 16 wherein the extreme-frequency channel has the lowest-corresponding frequency, and the extreme-capacitance combination of varactors provides the highest-capacitance amount available.